# YeaCreate-RK3566 Cord Board

## --Specification Sheet V1.0

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|---|---|
| Mainboard Model: | YeaCreate-RK3566-CORE V1.0 |
| Board Name: | YeaCreate-RK3566 Core Board |
| Security Level: | Public |

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| Reviewed by: | Simon |
| Approved by： | |

Release Date: 2026/6/5

# Directory

# 1. Introduction

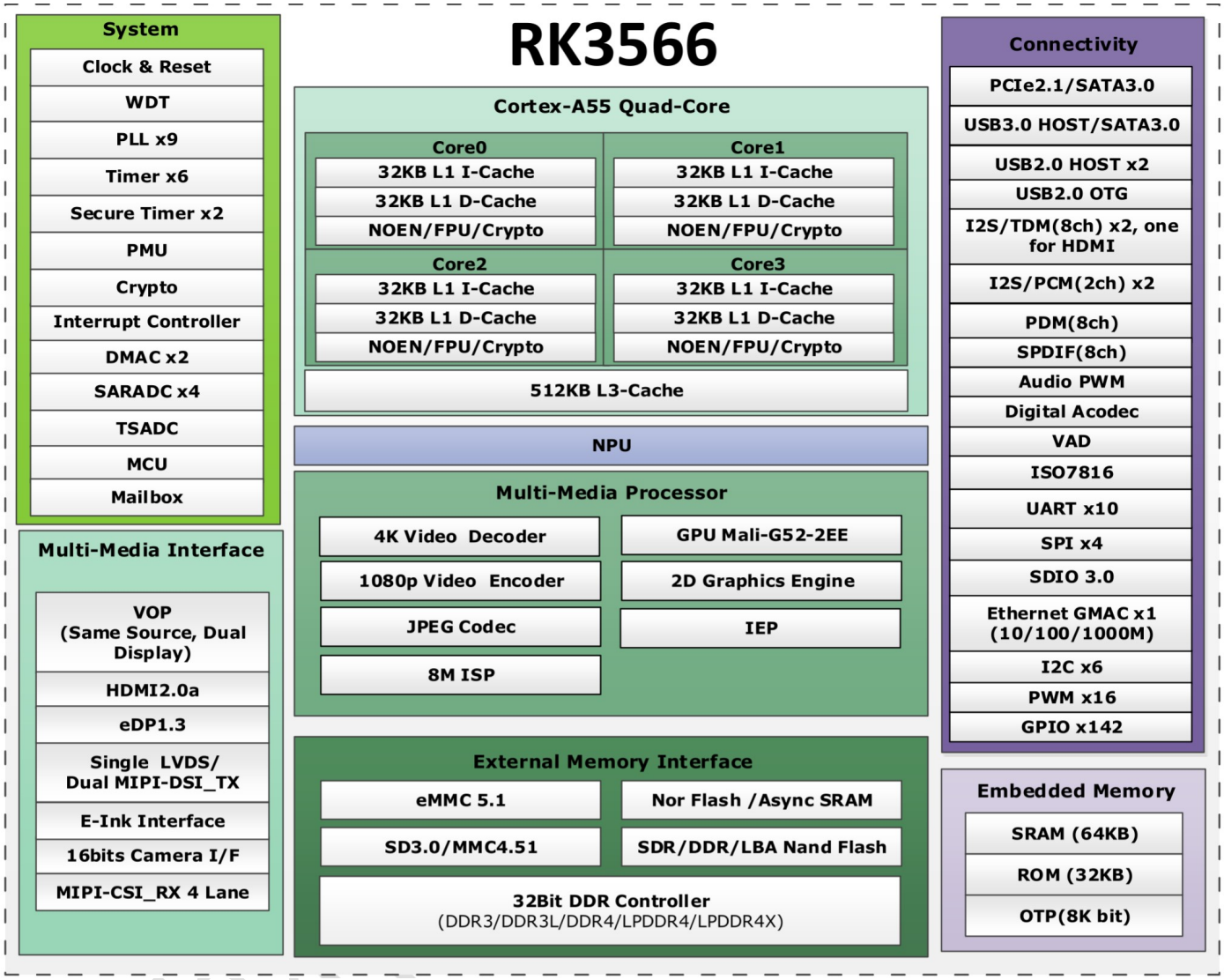
YeaCreate is dedicated to smart home solutions that create a wiser, more convenient life for people. As an innovator in embedded application technology, YeaCreate continuously drives innovation in home connectivity and intelligent interconnection solutions.

# 2. Features and Applications

1. The Core-RK3566 core board integrates the CPU, LPDDR4, eMMC, PMIC.
2. It features two display controllers supporting MIPI, LVDS, HDMI, and eDP interfaces. It supports up to dual independent displays or mirrored displays, with the HDMI output supporting up to 4K resolution.
3. It features high-speed interfaces including USB 3.0, PCIe 2.1, SDIO 3.0, SPI, and I²C for seamless peripheral connectivity.
4. It features a built-in NPU delivering up to 0.8 TOPS of computing power. It supports the Rockchip RKNN toolkit and mainstream frameworks such as TensorFlow and Caffe, meeting the demands of lightweight edge computing.
5. It supports application development across multiple platforms, including embedded Linux, Ubuntu, Debian, and Android.
6. Designed with a cord board and carries board architecture, the core board serves as the minimum system, while the carrier board handles peripheral interfaces. This allows for rapid development and verification using only a 2 - 4 layer carrier board.
7. The core board supports fast customization with different capacities of DRAM or EMMC.
8. The core board has been adapted with over 10 types of Wi-Fi modules.
9. A reserved shield case interface is provided for reliable operation in harsh environments.
10. High performance, low power consumption, and strong scalability. Highly integrated with a DDR4 gold finger package for easy installation. Proven stable and reliable through extensive deployment in diverse industrial embedded applications.

## 2.1. Functional Block Diagram

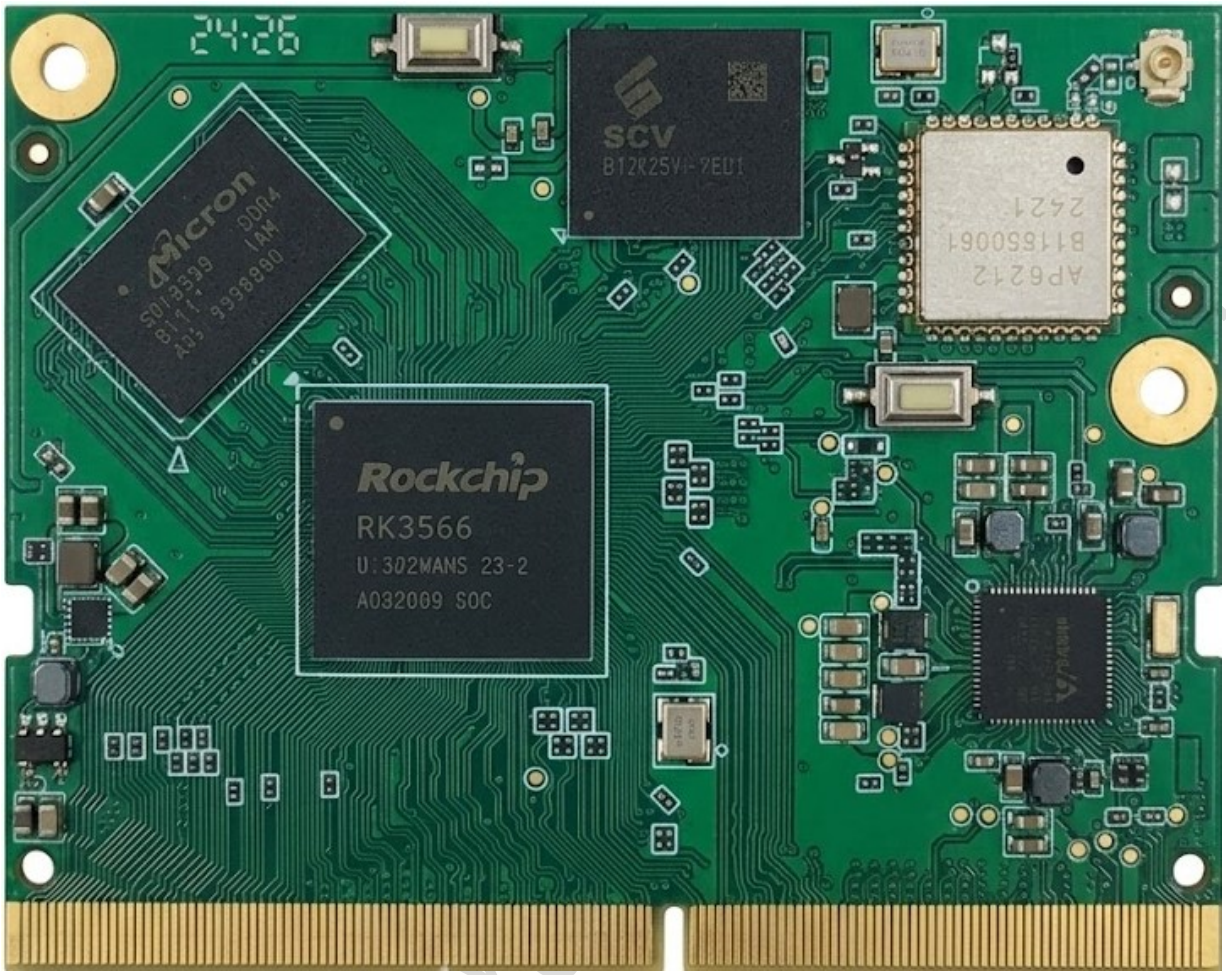
The Core-RK3566 Standard SoM utilizes the RK3566 as its main CPU. The functional block diagram of the chip is shown below:



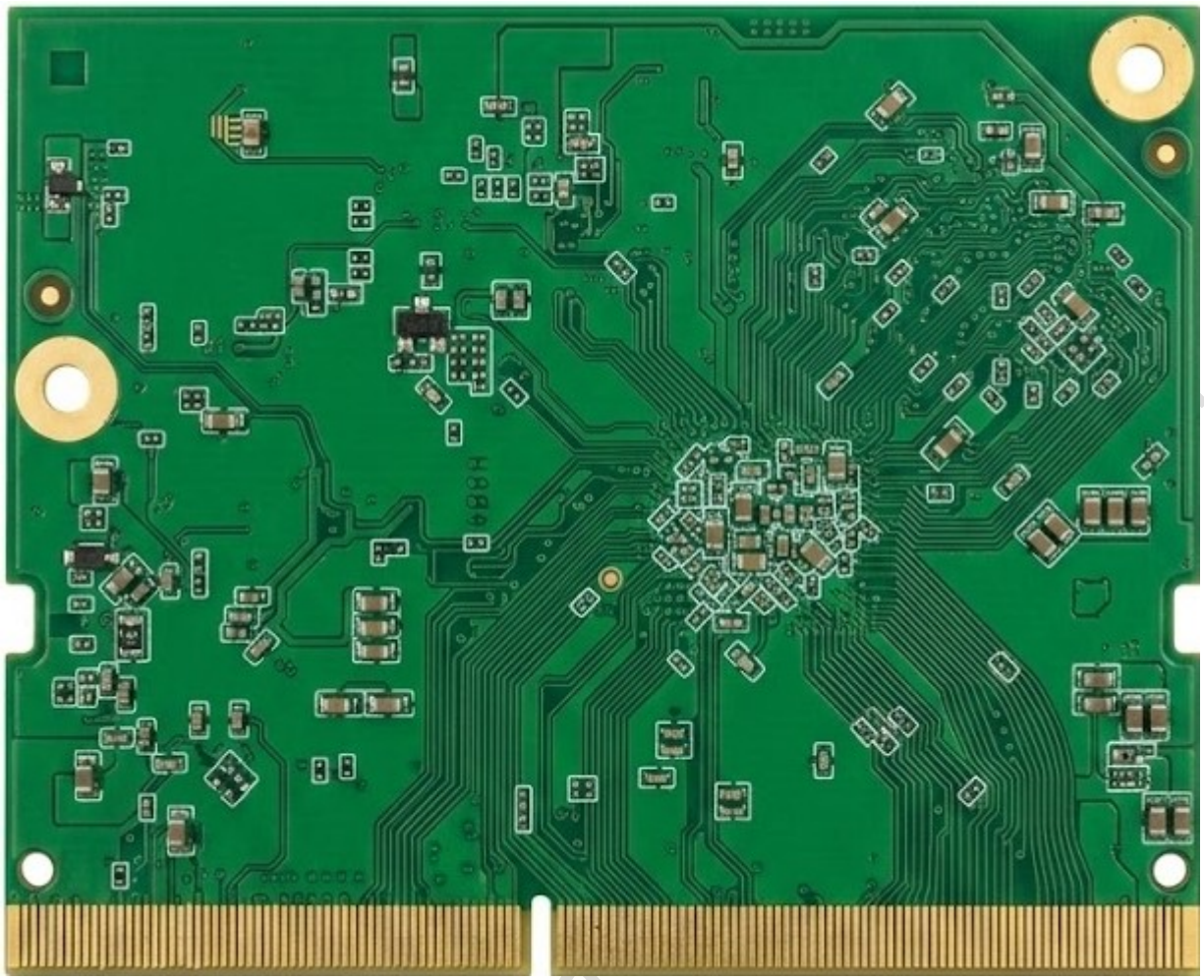
## 2.2. Applications

# 3. Mechanical Dimensions

## 3.1. Top View:



## 3.2 Bottom View:



## 3.3. Dimensions:

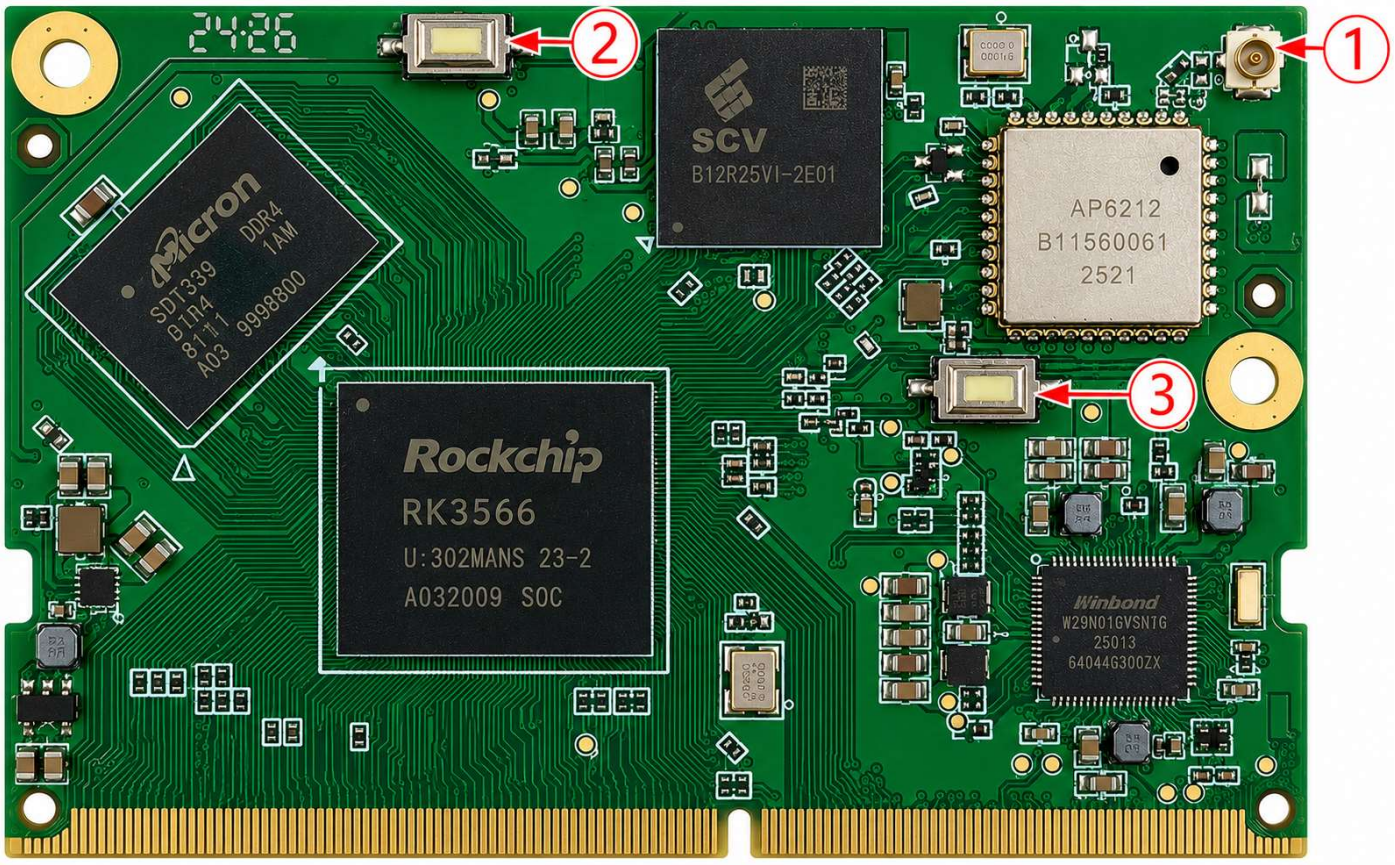
| | |
|---|---|
| Width | 55mm |
| Length | 69.5mm |
| Tolerance | ±0.5mm |

# 4. Electrical Characteristics

## 4.1.The basic parameters are listed in the table below:

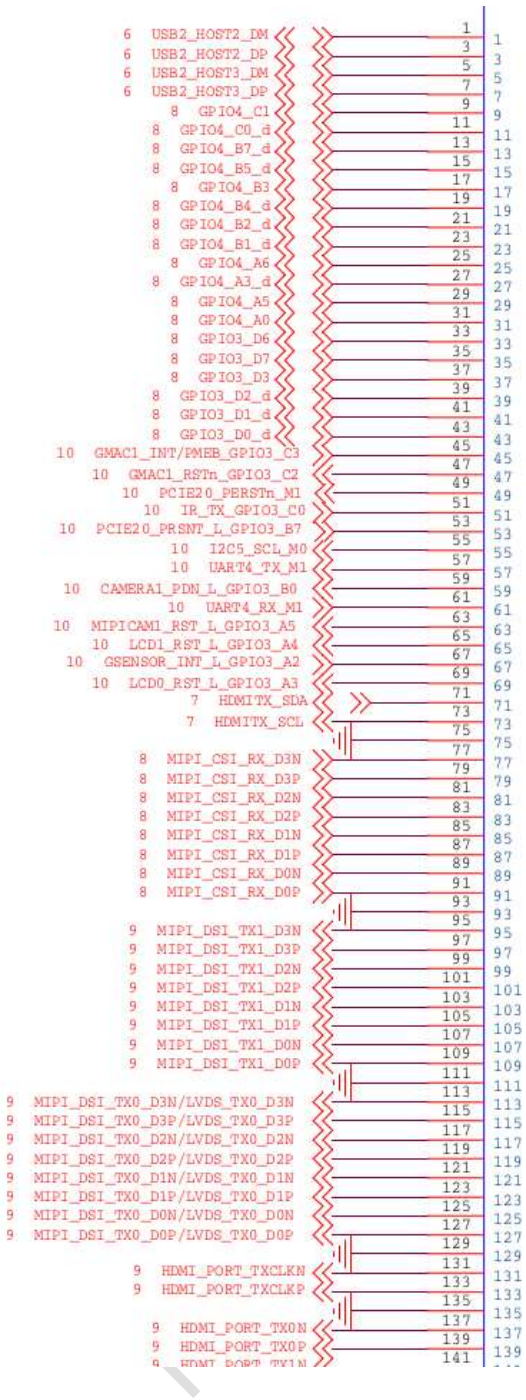
| Basic Parameters | |
|---|---|
| SoC | RockChip RK3566 |
| CPU | Quad-core 64-bit ARM Cortex-A55 processor, up to 1.8 GHz |
| GPU | Mali-G52 1-Core-2EE<br>Supporting OpenGL ES 1.1/2.0/3.2, OpenCL 2.0, Vulkan 1.1<br>Integrated high-performance 2D graphics acceleration hardware. |
| NPU | Neural network acceleration engine delivering up to 1 TOPS of processing power.<br>Supports hybrid INT8/INT16/FP16/BFP16 MAC operations.<br>Compatible with mainstream deep learning frameworks including TensorFlow, TF-Lite, PyTorch, Caffe, ONNX, MXNet, Keras, and Darknet. |
| Memory | LPDDR4/LPDDR4x, default 2GB |
| Storage | EMMC, default 32GB |
| Ethernet | Integrates a GMAC controller, providing a high-performance Gigabit Ethernet interface (1000 Mbps). |
| Multimedia | Supports 4K @ 60 fps video decoding (H.264, H.265, VP9).<br>Supports 1080p @ 100 fps video encoding (H.264, H.265).<br>Supports 8MP ISP. |
| Display Interface | Single display supported: eDP, HDMI 2.0, MIPI-DSI, LVDS, and EBC. |
| Audio Interface | 1 × HDMI audio output<br>1 × HPR/L, Stereo Headphone Output<br>1 × SPK, Amplifier Output<br>1 × MIC Microphone Inputs<br>1 × VAD |
| USB | 1 × USB2.0 OTG<br>1 × USB3.0 HOST<br>2 × USB2.0 HOST |
| PCIe/SATA | 1 × PCIe 2.0<br>2 × SATA 3.0 |
| Expansion Connector | 10 × UART<br>4 × SPI<br>5 × I2C<br>3 × I2S<br>3 × SDIO<br>16 × PWM<br>4 × ADC<br>1 × FSPI<br>116 × GPIO |

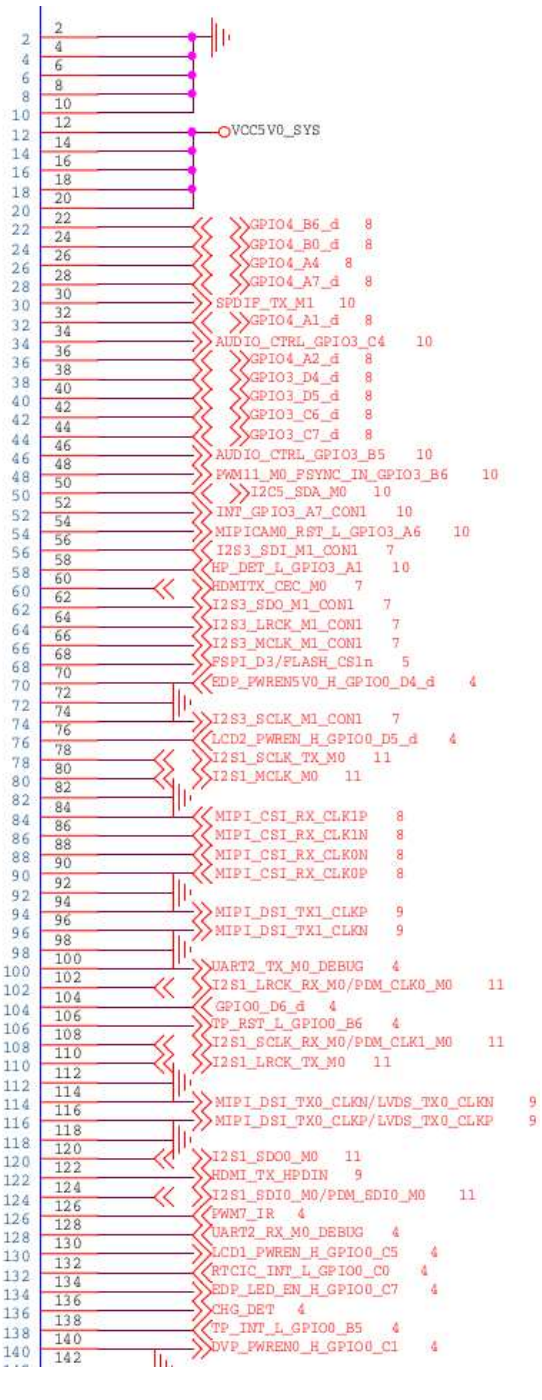
## 4.2. Core Board Functions:




| No. | Description |
|---|---|
| 1 | IPEX Gen 1 Connector |
| 2 | RK3566 BOOT Button |
| 3 | RK3566 Reset Button |

# 5. Pin Configuration and Functions




## 5.1. Core Board Interface – Odd Pin Definitions (Refer to the SoC Datasheet for detailed pin multiplexing functions.)

| Pin No. | Connector Label | Description |
|---|---|---|
| 1 | USB2_HOST2_DM | USB2_HOST2_DM |
| 3 | USB2_HOST2_DP | USB2_HOST2_DP |
| 5 | USB2_HOST3_DM | USB2_HOST3_DM |
| 7 | USB2_HOST2_DP | USB2_HOST2_DP |
| 9 | GPIO4_C1_d | GPIO4_C1_d |
| 11 | GPIO4_C0_d | GPIO4_C0_d |
| 13 | GPIO4_B7_d | GPIO4_B7_d |
| 15 | GPIO4_B5_d | GPIO4_B5_d |
| 17 | GPIO4_B3 | GPIO4_B3_d |
| 19 | GPIO4_B4_d | GPIO4_B4_d |
| 21 | GPIO4_B2_d | GPIO4_B2_d |
| 23 | GPIO4_B1_d | GPIO4_B1_d |
| 25 | GPIO4_A6 | GPIO4_A6_d |

| | | |
|---|---|---|
| 27 | GPIO4_A3_d | GPIO4_A3_d |
| 29 | GPIO4_A5 | GPIO4_A5_d |
| 31 | GPIO4_A0 | GPIO4_A0_d |
| 33 | GPIO3_D6 | GPIO3_D6_d |
| 35 | GPIO3_D7 | GPIO3_D7_d |
| 37 | GPIO3_D3 | GPIO3_D3_d |
| 39 | GPIO3_D2_d | GPIO3_D2_d |
| 41 | GPIO3_D1_d | GPIO3_D1_d |
| 43 | GPIO3_D0_d | GPIO3_D0_d |
| 45 | GMAC1_INT/PMEB_GPIO3_C3 | GPIO3_C3_d |
| 47 | GMAC1_RSTn_GPIO3_C2 | GPIO3_C2_d |
| 49 | PCIE20_PERSTn_M1 | GPIO3_C1_d |
| 51 | IR_TX_GPIO3_C0 | GPIO3_C0_d |
| 53 | PCIE20_PRSNT_L_GPIO3_B7 | GPIO3_B7_d |
| 55 | I2C5_SCL_M0 | I2C5 Clock Signal |
| 57 | UART4_TX_M1 | UART4 Transmit Data |
| 59 | CAMERA1_PDN_L_GPIO3_B0 | GPIO3_B0_d |
| 61 | UART4_RX_M1 | UART4 Receive Data |
| 63 | MIPICAM1_RST_L_GPIO3_A5 | GPIO3_A5_d |
| 65 | LCD1_RST_L_GPIO3_A4 | GPIO3_A4_d |
| 67 | GSENSOR_INT_L_GPIO3_A2 | GPIO3_A2_d |
| 69 | LCD0_RST_L_GPIO3_A3 | GPIO3_A3_d |
| 71 | HDMITX_SDA | |
| 73 | HDMITX_SCL | |
| 75 | GND | GND |
| 77 | MIPI_CSI_RX_D3N | MIPI_CSI_RX_D3N |
| 79 | MIPI_CSI_RX_D3P | MIPI_CSI_RX_D3P |
| 81 | MIPI_CSI_RX_D2N | MIPI_CSI_RX_D2N |
| 83 | MIPI_CSI_RX_D2P | MIPI_CSI_RX_D2P |
| 85 | MIPI_CSI_RX_D1N | MIPI_CSI_RX_D1N |
| 87 | MIPI_CSI_RX_D1P | MIPI_CSI_RX_D1P |
| 89 | MIPI_CSI_RX_D0N | MIPI_CSI_RX_D0N |
| 91 | MIPI_CSI_RX_D0P | MIPI_CSI_RX_D0P |
| 93 | GND | GND |
| 95 | MIPI_DSI_TX1_D3N | MIPI_DSI_TX1_D3N |
| 97 | MIPI_DSI_TX1_D3P | MIPI_DSI_TX1_D3P |
| 99 | MIPI_DSI_TX1_D2N | MIPI_DSI_TX1_D2N |
| 101 | MIPI_DSI_TX1_D2P | MIPI_DSI_TX1_D2P |
| 103 | MIPI_DSI_TX1_D1N | MIPI_DSI_TX1_D1N |
| 105 | MIPI_DSI_TX1_D1P | MIPI_DSI_TX1_D1P |
| 107 | MIPI_DSI_TX1_D0N | MIPI_DSI_TX1_D0N |
| 109 | MIPI_DSI_TX1_D0P | MIPI_DSI_TX1_D0P |
| 111 | GND | GND |
| 113 | MIPI_DSI_TX0_D3N/LVDS_TX0_D3N | Data Lane 3 Negative D3- |

| | | |
|---|---|---|
| 115 | MIPI_DSI_TX0_D3P/LVDS_TX0_D3P | Data Lane 3 Positive D3+ |
| 117 | MIPI_DSI_TX0_D2N/LVDS_TX0_D2N | Data Lane 2 Negative D2- |
| 119 | MIPI_DSI_TX0_D2P/LVDS_TX0_D2P | Data Lane 2 Positive D2+ |
| 121 | MIPI_DSI_TX0_D1N/LVDS_TX0_D1N | Data Lane 1 Negative D1- |
| 123 | MIPI_DSI_TX0_D1P/LVDS_TX0_D1P | Data Lane 1 Positive D1+ |
| 125 | MIPI_DSI_TX0_D0N/LVDS_TX0_D0N | Data Lane 0 Negative D0- |
| 127 | MIPI_DSI_TX0_D0P/LVDS_TX0_D0P | Data Lane 0 Positive D0+ |
| 129 | GND | GND |
| 131 | HDMI_PORT_TXCLKN | HDMI_TXCLK- |
| 133 | HDMI_PORT_TXCLKP | HDMI_TXCLK+ |
| 135 | GND | GND |
| 137 | HDMI_PORT_TX0N | HDMI_TX0- |
| 139 | HDMI_PORT_TX0P | HDMI_TX0+ |
| 141 | HDMI_PORT_TX1N | HDMI_TX1- |
| 143 | HDMI_PORT_TX1P | HDMI_TX1+ |
| 145 | HDMI_PORT_TX2N | HDMI_TX2- |
| 147 | HDMI_PORT_TX2P | HDMI_TX2+ |
| 149 | GND | GND |
| 151 | PCIE20_RXP | PCIE20_RX+ |
| 153 | PCIE20_RXN | PCIE20_RX- |
| 155 | PCIE20_TXN | PCIE20_TX- |
| 157 | PCIE20_TXP | PCIE20_TX+ |
| 159 | GND | GND |
| 161 | USB3_HOST1_SSTXP | USB3_HOST1_SSTX+ |
| 163 | USB3_HOST1_SSTXN | USB3_HOST1_SSTX- |
| 165 | USB3_HOST1_SSRXP | USB3_HOST1_SSRX+ |
| 167 | USB3_HOST1_SSRXN | USB3_HOST1_SSRX- |
| 169 | USB_OTG0_VBUSDET | USB_OTG0_VBUS Detect |
| 171 | GND | GND |
| 173 | EDP_TX_AUXP | EDP_TX_AUX+ |
| 175 | EDP_TX_AUXN | EDP_TX_AUX- |
| 177 | GND | GND |
| 179 | EDP_TX_D0P | EDP_TX_D0+ |
| 181 | EDP_TX_D0N | EDP_TX_D0- |
| 183 | EDP_TX_D1P | EDP_TX_D1+ |
| 185 | EDP_TX_D1N | EDP_TX_D1- |
| 187 | EDP_TX_D3N | EDP_TX_D3- |
| 189 | EDP_TX_D3P | EDP_TX_D3+ |
| 191 | EDP_TX_D2P | EDP_TX_D2+ |
| 193 | EDP_TX_D2N | EDP_TX_D2- |
| 195 | GND | GND |
| 197 | I2S1_SDO3_M0/I2S1_SDI1_M0/PDM_SDI1_M0 | GPIO1_B2_d |
| 199 | eMMC_RSTn/FSPI_D2/FLASH_WPn | GPIO1_C7_d |

| | | |
|---|---|---|
| 201 | I2S1_SDO1_M0/I2S1_SDI3_M0/PDM_SDI3_M0 | GPIO1_B0_d |
| 203 | I2C3_SCL_M0 | I2C3 Clock Signal |
| 205 | GND | GND |
| 207 | SDMMC0_CLK/TEST_CLKOUT/UART5_TX_M0 | SDMMC0 Clock Signal |
| 209 | I2C3_SDA_M0 | I2C3 Data Signal |
| 211 | FSPI_CLK/FLASH_ALE | GPIO1_D0_d |
| 213 | I2C1_SDA_TP | I2C1 Data Signal |
| 215 | LCD0_BL_PWM4 | GPIO0_C3_d |
| 217 | SDMMC0_DET_L | SDMMC0_DET_L |
| 219 | FSPI_D0/FLASH_RDY | GPIO1_D1 |
| 221 | VCC_3V3 | VCC_3V3 |
| 223 | VCC_3V3 | VCC_3V3 |
| 225 | GND | GND |
| 227 | VCC3V3_RTC | VCC3V3_RTC |
| 229 | VCC_1V8 | VCC_1V8 |
| 231 | VCC_1V8 | VCC_1V8 |
| 233 | GND | GND |
| 235 | GND | GND |
| 237 | I2S1_SDO2_M0/I2S1_SDI2_M0/PDM_SDI2_M0 | GPIO1_B1_d |
| 239 | USB_OTG_PWREN_H_GPIO0_A5 | GPIO0_A5_d |
| 241 | PMIC_EXT_EN | PMIC_EXT_EN |
| 243 | VCC3V3_SD | VCC3V3_SD |
| 245 | VCC3V3_SD | VCC3V3_SD |
| 247 | MIC1_INP | Microphone 1 Positive (Mic+) |
| 249 | MIC1_INN | Microphone 1 Negative (Mic-) |
| 251 | HPL_OUT | Headphone Left Channel Output |
| 253 | EDP_BL_PWM5 | GPIO0_C4_d |
| 255 | HPR_OUT | Headphone Right Channel Output |
| 257 | VBAT_SNSP | VBAT_SNSP |
| 259 | VBAT_SNSN | VBAT_SNSN |
| | | |

## 5.2. Core Board Interface – Even Pin Definitions (Refer to the SoC Datasheet for detailed pin multiplexing functions.)

| Pin No. | Connector Label | Description |
|---|---|---|
| 2 | GND | GND |
| 4 | GND | GND |
| 6 | GND | GND |
| 8 | GND | GND |
| 10 | GND | GND |

| | | |
|---|---|---|
| 12 | VCC5V0_SYS | VCC5V0_SYS |
| 14 | VCC5V0_SYS | VCC5V0_SYS |
| 16 | VCC5V0_SYS | VCC5V0_SYS |
| 18 | VCC5V0_SYS | VCC5V0_SYS |
| 20 | GVCC5V0_SYS | VCC5V0_SYS |
| 22 | GPIO4_B6_d | GPIO4_B6_d |
| 24 | GPIO4_B0_d | GPIO4_B0_d |
| 26 | GPIO4_A4 | GPIO4_A4_d |
| 28 | GPIO4_A7_d | GPIO4_A7_d |
| 30 | SPDIF_TX_M1 | SPDIF_TX_M1 |
| 32 | GPIO4_A1_d | GPIO4_A1_d |
| 34 | AUDIO_CTRL_GPIO3_C4 | GPIO3_C4_d |
| 36 | GPIO4_A2_d | GPIO4_A2_d |
| 38 | GPIO3_D4_d | GPIO3_D4_d |
| 40 | GPIO3_D5_d | GPIO3_D5_d |
| 42 | GPIO3_C6_d | GPIO3_C6_d |
| 44 | GPIO3_C7_d | GPIO3_C7_d |
| 46 | AUDIO_CTRL_GPIO3_B5 | AUDIO_CTRL_GPIO3_B5 |
| 48 | PWM11_M0_FSYNC_IN_GPIO3_B6 | GPIO3_B6_d |
| 50 | I2C5_SDA_M0 | SDA Data Signal |
| 52 | INT_GPIO3_A7_CON1 | GPIO3_A7_d |
| 54 | MIPICAM0_RST_L_GPIO3_A6 | GPIO3_A6_d |
| 56 | I2S3_SDI_M1_CON1 | GPIO4_C6_d |
| 58 | HP_DET_L_GPIO3_A1 | GPIO3_A1_d |
| 60 | HDMITX_CEC_M0 | HDMITX_CEC Signal |
| 62 | I2S3_SDO_M1_CON1 | GPIO4_C5_d |
| 64 | I2S3_LRCK_M1_CON1 | GPIO4_C4_d |
| 66 | I2S3_MCLK_M1_CON1 | GPIO4_C2_d |
| 68 | FSPI_D3/FLASH_CS1n | GPIO1_D4 |
| 70 | EDP_PWREN5V0_H_GPIO0_D4_d | GPIO0_D4_d |
| 72 | GND | GND |
| 74 | I2S3_SCLK_M1_CON1 | GPIO4_C3_d |
| 76 | LCD2_PWREN_H_GPIO0_D5_d | GPIO0_D5_d |
| 78 | I2S1_SCLK_TX_M0 | GPIO1_A3_d |
| 80 | I2S1_MCLK_M0 | GPIO1_A2_d |
| 82 | GND | GND |
| 84 | MIPI_CSI_RX_CLK1P | CSI Clock Lane 1 Positive 1+ |
| 86 | MIPI_CSI_RX_CLK1N | CSI Clock Lane 1 Negative 1- |
| 88 | MIPI_CSI_RX_CLK0N | CSI Clock Lane 0 Negative 0- |
| 90 | MIPI_CSI_RX_CLK0P | CSI Clock Lane 0 Positive 0+ |
| 92 | GND | GND |
| 94 | MIPI_DSI_TX1_CLKP | Clock Lane Positive CLK+ |
| 96 | MIPI_DSI_TX1_CLKN | Clock Lane Negative CLK- |
| 98 | GND | GND |

| | | |
|---|---|---|
| 100 | UART2_TX_M0_DEBUG | UART2 Debug Transmit Data |
| 102 | I2S1_LRCK_RX_M0/PDM_CLK0_M0 | GPIO1_A6_d |
| 104 | GPIO0_D6_d | GPIO0_D6_d |
| 106 | TP_RST_L_GPIO0_B6 | GPIO0_B6 |
| 108 | I2S1_SCLK_RX_M0/PDM_CLK1_M0 | GPIO1_A4_d |
| 110 | I2S1_LRCK_TX_M0 | GPIO1_A5_d |
| 112 | GND | GND |
| 114 | MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN | Clock Lane Negative CLK- |
| 116 | MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP | Clock Lane Positive CLK+ |
| 118 | GND | GND |
| 120 | I2S1_SDO0_M0 | GPIO1_A7_d |
| 122 | HDMI_TX_HPDIN | HDMI Hot Plug Detect |
| 124 | I2S1_SDI0_M0/PDM_SDI0_M0 | GPIO1_B3_d |
| 126 | PWM7_IR | GPIO0_C6_d |
| 128 | UART2_RX_M0_DEBUG | UART2 Debug Receive Data |
| 130 | LCD1_PWREN_H_GPIO0_C5 | GPIO0_C5_d |
| 132 | RTCIC_INT_L_GPIO0_C0 | GPIO0_C0_d |
| 134 | EDP_LED_EN_H_GPIO0_C7 | GPIO0_C7_d |
| 136 | CHG_DET | GPIO0_B0 |
| 138 | TP_INT_L_GPIO0_B5 | GPIO0_B5 |
| 140 | DVP_PWREN0_H_GPIO0_C1 | GPIO0_C1_d |
| 142 | GND | GND |
| 144 | INT#_SENSOR | GPIO0_B7_d |
| 146 | REFCLK_OUT_CAM | GPIO0_A0_d |
| 148 | GND | GND |
| 150 | PCIE20_REFCLKP | PCIE20_REFCLK+ |
| 152 | PCIE20_REFCLKN | PCIE20_REFCLK- |
| 154 | GND | GND |
| 156 | USB3_HOST1_DP | USB3_HOST1+ |
| 158 | USB3_HOST1_DM | USB3_HOST1- |
| 160 | GND | GND |
| 162 | USB_OTG0_DM | USB_OTG0- |
| 164 | USB_OTG0_DP | USB_OTG0+ |
| 166 | SDMMC0_D1/UART2_RX_M1/UART6_RX_M1/PWM9_M1 | SDMMC0 Data 1 |
| 168 | SDMMC0_D3/ARM_JTAG_TMS | SDMMC0 Data 3 |
| 170 | SDMMC0_CMD/PWM10_M1/UART5_RX_M0 | SDMMC0 Command Signal |
| 172 | SDMMC0_D0/UART2_TX_M1/UART6_TX_M1/PWM8_M1 | SDMMC0 Data 0 |
| 174 | B_RK809_32KOUT_WIFI | RK809 32.768kHz Clock Output |
| 176 | SDMMC0_D2/ARM_JTAG_TCK | SDMMC0 Data 2 |
| 178 | VCC_BAT | VCC_BAT |
| 180 | B_SOC_PCM_OUT | B_SOC_PCM_OUT |

| | | |
|---|---|---|
| 182 | B_SOC_PCM_IN | B_SOC_PCM_IN |
| 184 | SARADC_VIN3 | SARADC_VIN3 |
| 186 | SARADC_VIN0_KEY/RECOVERY | RECOVERY Firmware Upgrade |
| 188 | B_SOC_PCM_CLK | B_SOC_PCM_CLK |
| 190 | SARADC_VIN2_LCD_ID | SARADC_VIN2_LCD_ID |
| 192 | I2S1_SDO0_M0_RK809 | I2S1_SDO0_M0_RK809 |
| 194 | I2S1_SDI0_M0/PDM_SDI0_M0_RK809 | I2S1_SDI0_M0/PDM_SDI0_M0_RK809 |
| 196 | SARADC_VIN1_EVB_HW_ID | SARADC_VIN1_EVB_HW_ID |
| 198 | USB_OTG0_ID | USB_OTG0_ID Signal |
| 200 | PDM_CLK0_M0_RK809 | PDM_CLK0_M0_RK809 |
| 202 | B_SOC_PCM_SYNC | GPIO2_C3_d |
| 204 | I2S1_LRCK_TX_M0_RK809 | I2S1_LRCK_TX_M0_RK809 |
| 206 | I2S1_SCLK_TX_M0_RK809 | I2S1_SCLK_TX_M0_RK809 |
| 208 | I2S1_MCLK_M0_RK809 | I2S1_MCLK_M0_RK809 |
| 210 | I2C1_SCL_TP | I2C Clock Signal |
| 212 | RESETn | Reset Input |
| 214 | EDP_HDPIN_GPIO0_C2 | GPIO0_C2_d |
| 216 | FSPI_D1/FLASH_RDn | GPIO1_D2 |
| 218 | FSPI_CS0n/FLASH_CS0n | GPIO1_D3 |
| 220 | VCC_3V3 | VCC_3V3 |
| 222 | VCC_3V3 | VCC_3V3 |
| 224 | GND | GND |
| 226 | RK809_PWRON | Power On/Off Control |
| 228 | VCC_1V8 | VCC_1V8 |
| 230 | VCC_1V8 | VCC_1V8 |
| 232 | GND | GND |
| 234 | VCCIO_ACODEC | VCCIO_ACODEC |
| 236 | GND | GND |
| 238 | PCIE_PWREN_H_GPIO0_A6 | GPIO0_A6_d |
| 240 | VCCIO_SD | VCCIO_SD |
| 242 | SPKP_OUT | SPK+ Speaker Positive Output |
| 244 | SPKN_OUT | SPK- Speaker Negative Output |
| 246 | GND | GND |
| 248 | GND | GND |
| 250 | HP_SNS | HP_SNS |
| 252 | VCC3V3_PMU | VCC3V3_PMU |
| 254 | VCC3V3_PMU | VCC3V3_PMU |
| 256 | VCC5V0_SYS | VCC5V0_SYS |
| 258 | VCC5V0_SYS | VCC5V0_SYS |
| 260 | VCC5V0_SYS | VCC5V0_SYS |